REMARKS

The Examiner rejected Claims 1-10 under 35 U.S.C. 112, first paragraph, because the Examiner maintains that the chemical reactions used in CMP are unpredictable chemical reactions. Applicant disagrees, more than 8000 patents were granted to processes using CMP in the decade prior to the filing of this application. The precise chemical reactions used in these processes are often not included in the specifications of those patents. Hence, the Patent Office has already determined that CMP is sufficiently predicable. However, the above amendment to Claims 1 and 7 remove the "chemical" part of the polishing operation, and hence, renders this issue moot.

The Examiner rejected Claims 1-3 and 5-7 under 35 U.S.C. 102(e) as being anticipated by Schrems (US 2002/0125521). Applicant submits that these claims as amended above are not anticipated by Schrems.

In making this rejection, the Examiner points to the hole in which the capacitor is formed as the via. First, the capacitors in question are integrated circuit elements. In particular, the outer layer 310 that the Examiner identifies as the stop material is the outer electrode of the capacitor. Hence, the vias do not extend below the integrated circuit elements as now required by Claims 1 and 7.

With reference to Claim 3, the Examiner points to layer 164 as the electrically insulating layer that lines the via. Applicant must disagree. Even with the Examiner's definition of the via, the via is lined with layer 310 which is a conducting material. Accordingly there are additional grounds for allowing Claim 3.

The Examiner rejected Claims 1-3 and 7-10 under 35 U.S.C. 102(b) as being anticipated by Clements (US 4,054,875). Applicant submits that these claims as amended above are not anticipated by Clements.

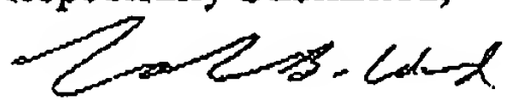
In making this rejection, the Examiner identifies wafer 10 as the substrate having a first and second surface. The Examiner looks to the layer shown at 40 in Figure 9 as the stop layer. The Examiner states that this stop layer lines the via. First, the via in question extends completely through the substrate at the point that layer 40 is applied. Hence, layer 40 does not cover the bottom of the via. Furthermore, since the via extends completely through the substrate, the via fails to satisfy the condition that its depth is less than the thickness of the substrate. Accordingly, Applicant submits that the Examiner has not made a *primia facia* case for anticipation with reference to Claims 1, 7, and the claims dependent therefrom.

The Examiner rejected Claim 4 under 35 U.S.C. 103(a) as being unpatentable over Schrems (US 2002/0125521). Applicant submits that this claim as amended above is not obvious in view of Schrems. Applicant repeats the arguments made above with respect to the elements missing from Schrems relative to Claims 1 and 3 from which Claim 4 depends.

In making this rejection, the Examiner admits that Schrems does not teach that the vias are lined with silicon dioxide. The Examiner states that silicon dioxide is known to the art. The Examiner maintains that Claim 8 of Schrems teaches an oxide layer, and hence, provides motivation for an oxide layer of silicon dioxide. The insulating web referred to in Claim 8 is element 320 of Figure 1 of Schrems. This element does not line the via identified by the Examiner. Hence, even if one were to make the replacement suggested by the Examiner, the resulting device would not satisfy the limitations of Claim 4. Accordingly, Applicant submits that the Examiner has not made a *primia facia* case for obviousness with respect to Claim 4.

I hereby certify that this paper is being sent by FAX to 703-872-9306.

Respectfully Submitted,



Calvin B. Ward
Registration No. 30,896
Date: April 1, 2004

18 Crow Canyon Court, Suite 305
San Ramon, CA 94583
Telephone (925) 855-0413 Telefax (925) 855-9214